Listing of Claims:

1. (Currently Amended) A method for providing field programmable platform array units, comprising:

cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units, said plurality of platform array units having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and interconnect between said plurality of platform array units being pre-routed on chip; and

packaging and testing said N by M array of platform array units;

wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal;

wherein said single platform array unit platform is a digital signal processing (DSP) platform.

2. (Original) The method of claim 1, further comprising:

programming said N by M array of platform array units by said customer.

3. (Original) The method of claim 2, wherein said programming is performed for at least one of unit specialization, unit role assignment, and inter-unit communications.

4. (Original) The method of claim 2, wherein said programming is performed with firmware.

5. (Canceled)

6. (Previously Presented) The method of claim 1, wherein said single platform array unit platform is a storage area network (SAN) platform.

7. (Canceled)

8. (Original) The method of claim 1, further comprising storing said field programmable platform array wafer.

9. (Currently Amended) A system for providing field programmable platform array units, comprising:

means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units, said plurality of platform array units having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and interconnect between said plurality of platform array units being pre-routed on chip; and

means for packaging and testing said N by M array of platform array units;

wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal;

wherein said single platform array unit platform is a digital signal processing (DSP) platform.

10. (Original) The system of claim 9, further comprising:

means for programming said N by M array of platform array units by said customer.

11. (Original) The system of claim 10, wherein said programming is performed for at least one of unit specialization, unit role assignment, and inter-unit communications.

12. (Original) The system of claim 10, wherein said programming is performed with firmware.

13. (Canceled)

14. (Previously Presented) The system of claim 9, wherein said single platform array unit platform is a storage area network (SAN) platform.

15. (Canceled)

16. (Original) The system of claim 9, further comprising means for storing said field programmable platform array wafer.

17. (Currently Amended) A semiconductor device, comprising:

a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor;

wherein interconnect between said plurality of platform array units being pre-routed;

wherein said single platform array unit platform is a digital signal processing (DSP) platform;

wherein encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal.

18. (Previously Presented) The semiconductor device of claim 17, wherein said semiconductor device includes top aluminum pads and said top aluminum pads of said semiconductor device are used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

19. (Canceled)

20. (Previously Presented) The semiconductor device of claim 17, wherein metal bumps of said semiconductor device are used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

21. (Previously Presented) The semiconductor device of claim 17, wherein a copper layer within said semiconductor device is used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

22. (Previously Presented) The semiconductor device of claim 17, wherein a polysilicon layer of said semiconductor device is used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

23. (Previously Presented) The semiconductor device of claim 17, wherein a silicon layer of said semiconductor device is used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

24. (Original) The semiconductor device of claim 17, wherein said plurality of platform array units are configured by external software programming.